UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,221	04/13/2004	Se-Hoon Oh	5649-1228	4644

20792 7590 10/10/2006

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,221	OH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-27* is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 6/01/06. Currently, claims 9-27 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 9-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zurcher et al., US Patent 6,500,724 in view of Admitted Prior Art.

Zurcher discloses the semiconductor method substantially as claimed. See figures 1 and 2, and corresponding text, where Zurcher shows, pertaining to claim 9, a method of forming an integrated circuit device comprising: forming a buried contact plug **38** on a cell array region of an integrated circuit substrate (figures 1 and 2; col. 2, lines 25-34); forming a resistor **32** on a peripheral circuit region of the integrated circuit substrate (figures 1 and 2; col. 2, lines 52-65);

forming a first pad contact plug **44** on the buried contact plug (figures 1 and 2; col. 3, lines 1-5); forming a second pad contact plug **42** on the resistor (figures 1 and 2; col. 3, lines 6-12); and forming a metal contact plug **44** on the second pad contact plug in the peripheral circuit region (figures 1 and 2; col. 3, lines 6-12). In addition, Zurcher shows, pertaining to claim 10, forming a capacitor **26/24/22/20** including in a lower electrode **20** on the first pad contact, a capacitor dielectric **22** on the lower electrode, and an upper electrode **24** on the capacitor dielectric layer. Also, Zurcher shows, pertaining to claim 11, wherein forming the capacitor **26/24/22/20** is preceded by: forming a lower interlayer dielectric layer **30** on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole **38** in the cell array region, wherein the buried contact plug **38** is disposed in the contact hole and wherein the resistor **32** is disposed on the lower interlayer dielectric layer (figure 1; col. 3, lines 1-15); and forming a first interlayer dielectric layer **34** on the lower interlayer dielectric layer, the buried contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole **38** in the cell array region and a second contact pad contact hole **42** in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively (figure 1; col. 3, lines 1-15). Zurcher shows, pertaining to claim 12, wherein forming the metal contact plug further comprises: forming a second interlayer dielectric layer **46** on the capacitor **26/24/22/20** and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole **44** in the peripheral circuit region (figure 1; col. 3, lines 10-15); and forming the metal contact plug **44** in the metal contact hole in the peripheral circuit region (figure 1; col. 3, lines 10-15). In addition, Zurcher shows, pertaining to claim 13,

further comprising forming an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer (col. 3, lines 16-26).

In addition, Zurcher shows, pertaining to claim 15, forming a first pad contact plug **44** and a buried contact plug **38** in a cell array region of an integrated circuit substrate and between a second pad contact plug **42** and a resistor **32** in a peripheral circuit region of the integrated circuit substrate (figures 1 and 2); and then forming a capacitor **26/24/22/20** on the first on the first pad contact plug in the cell array region of the integrated circuit substrate (figure 1); and forming a metal contact plug **44** on the second pad contact plug in the peripheral circuit region (figure 1 and 2). In addition, Zurcher shows, pertaining to claim 16, wherein forming the capacitor comprises: forming a lower electrode **20** on the first pad contact plug **44** (figure 1); forming a capacitor dielectric layer **22** on the lower electrode (figure 1); and forming an upper electrode **24** on the capacitor dielectric layer (figure 1). Also, Zurcher shows, pertaining to claim 17, wherein forming the capacitor is preceded by: forming the buried contact plug **38** on the cell array region of the integrated circuit substrate (figure 1); forming the resistor **32** on the peripheral circuit region of the integrated circuit substrate (figure 1); forming the first pad contact plug **44** on the buried contact plug in the cell array region (figure 1); and forming the second pad contact plug **44** on the resistor in the peripheral circuit region (figure 1). Zurcher shows, pertaining to claim 18, wherein forming the capacitor is further preceded by: forming a lower interlayer dielectric layer **22** on the integrated circuit substrate, wherein the lower interlayer dielectric layer defines a contact hole in the cell array region, wherein the buried contact plug is disposed in the contact hole and wherein the resistor **32** is disposed on the lower interlayer dielectric (figure 1); and forming a first interlayer dielectric layer **34** on the lower interlayer dielectric layer, the buried

contact plug and the resistor, wherein the first interlayer dielectric layer defines a first pad contact hole in the cell array region and a second pad contact hole in the peripheral circuit region and wherein the first and second pad contact plugs are disposed in the first and second pad contact holes, respectively (figure 1). In addition, Zurcher shows, pertaining to claim 19, wherein forming the metal contact plug further: forming a second interlayer dielectric layer **46** on the capacitor and the first interlayer dielectric layer, the second interlayer dielectric layer defining a metal contact hole in the peripheral circuit region; and forming the metal contact plug in the metal contact hole in the peripheral circuit region (figure 1). Finally, Zurcher shows, pertaining to claim 20, further comprising forming an etch stop layer between the first interlayer dielectric layer and the second interlayer dielectric layer (col.3, lines 15-20, silicon nitride is a none etch-stop material).

However, Zurcher fails to show, pertaining to claims 9 and 15, forming an ohmic contact layer between the first pad contact plug and the buried contact plug and between the second pad contact plug and the resistor. In addition, Zurcher fails to show, pertaining to claim 14, further comprising: forming a first adhesion layer between the first pad contact plug and the first interlayer dielectric layer, between the first pad contact plug and buried contact plug, between the second pad contact plug and the first interlayer dielectric layer, and between the second pad contact plug and the resistor; and forming a second adhesion layer between the metal contact plug and the second interlayer dielectric layer and between the metal contact plug and the second pad contact plug.

However, Zurcher fails to show, pertaining to claims 9 and 15, forming an ohmic layer between the first pad contact plug and the buried contact plug.

Admitted Prior Art teaches, that an ohmic layer can be formed at a bottom of a metal contact how to reduce the resistivity between the metal of the contact plug and the polysilicon of the resistor (page 2, lines 18-30).

It would have been obvious to one of ordinary skill in the art to incorporate, forming an ohmic layer between the first pad contact plug and the buried contact plug, in the method of Zurcher, pertaining to claims 9 and 15, according to the teachings of Admitted Prior Art, with the motivation that, by forming an ohmic layer the resistivity between the contact and the polysilicon layer would be greatly reduced, resulting in a more efficient electrical connection to the semiconductor device. In addition, pertaining to claim 14, it is conventional that adhesion layers are included within metal contact plugs to ad in the reliability of the contact and would result in routine experimentation.

Allowable Subject Matter

Claims 21-27 are allowed over the prior art of record (subjected to further search).

The following is an examiner's statement of reasons for allowance: The closest prior art of record, Zurcher et al., US Patent 6,500,724, fails to show the following step of:

Pertaining to independent claim 1, " patterning the first conductive layer to provide a buried contact plug in the contact hole in the cell array region and a resistor on the lower interlayer dielectric layer in a peripheral circuit region on the integrated circuit substrate;".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 9-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stanetta Isaac
Patent Examiner
September 25, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER